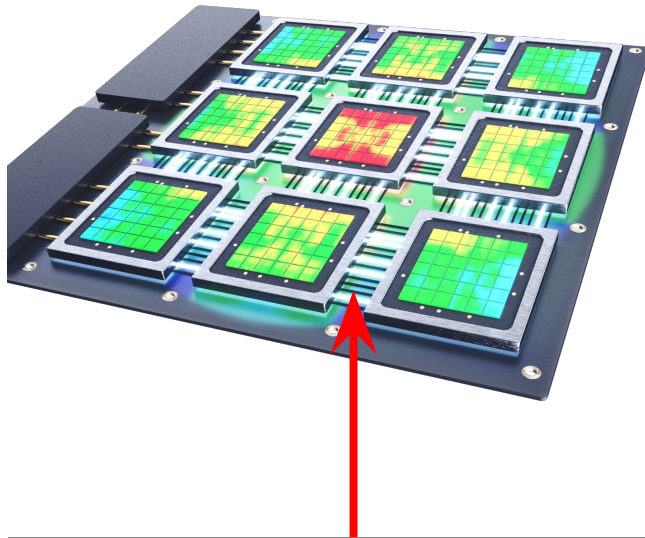


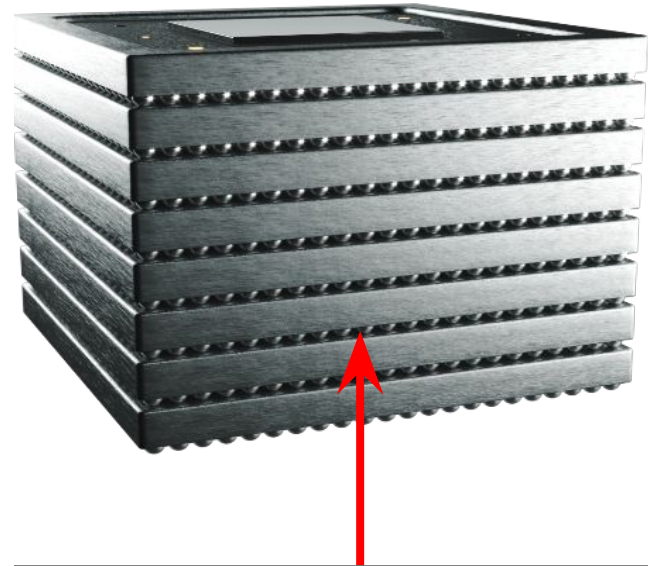


Heterogeneous Integration (HI) Part 1

Interconnects in Advanced Packaging



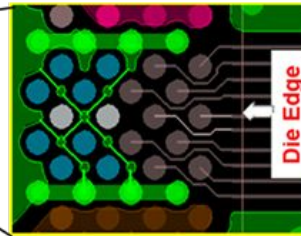
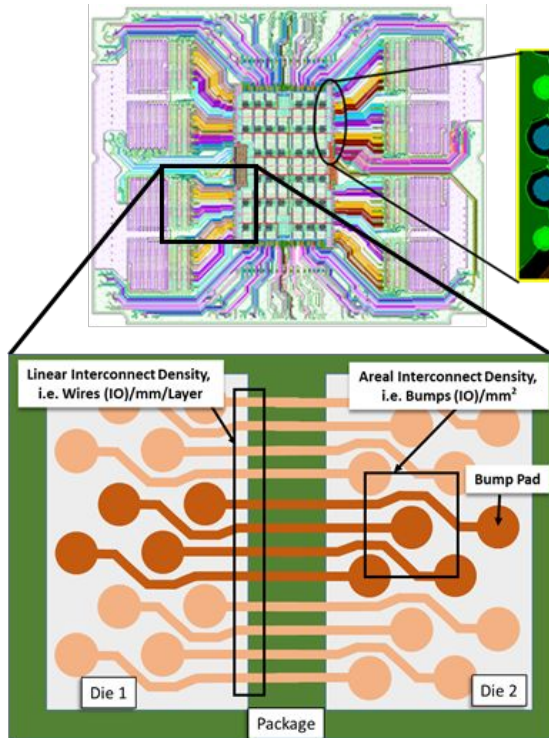
2D Interconnect



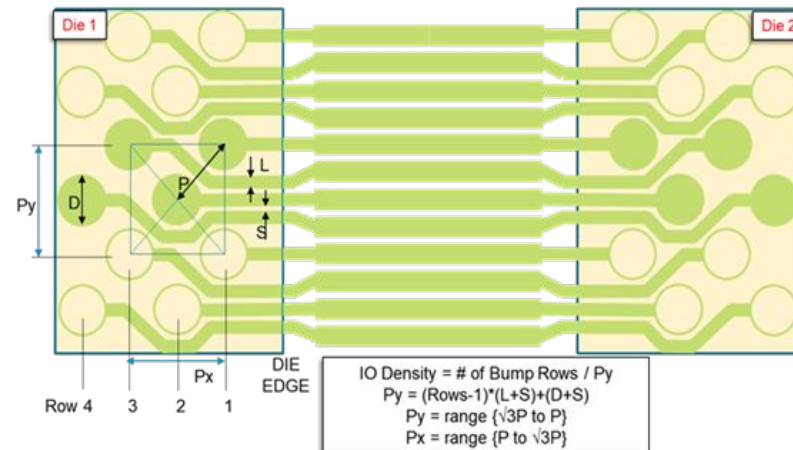
3D Interconnect

High Bandwidth, Low Power, Parallel Links require High Density Die-Die Interconnects - Driving Vision : SIP
Interconnects ~ SOC Interconnects

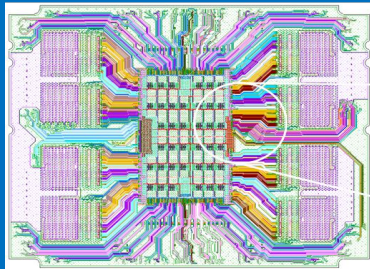
High Density Interconnects : Physical Metrics



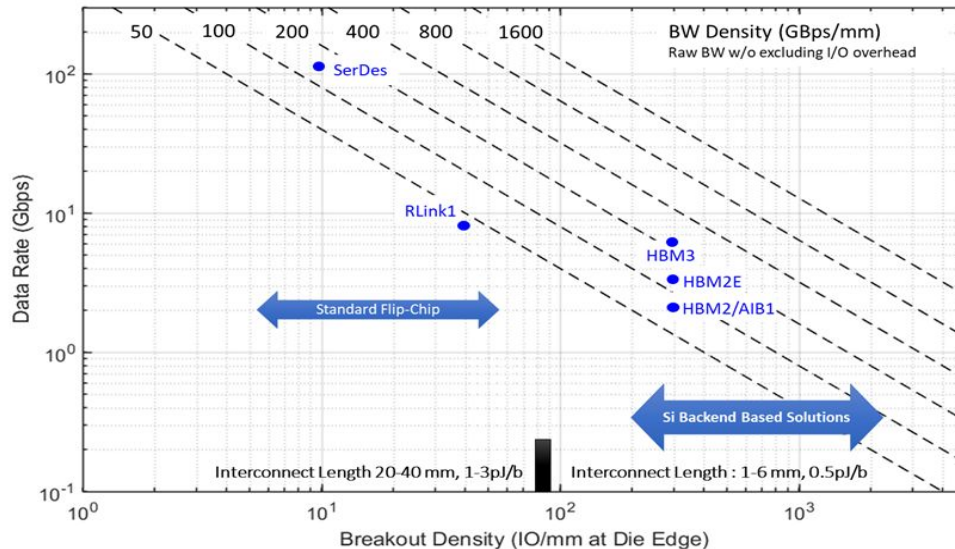
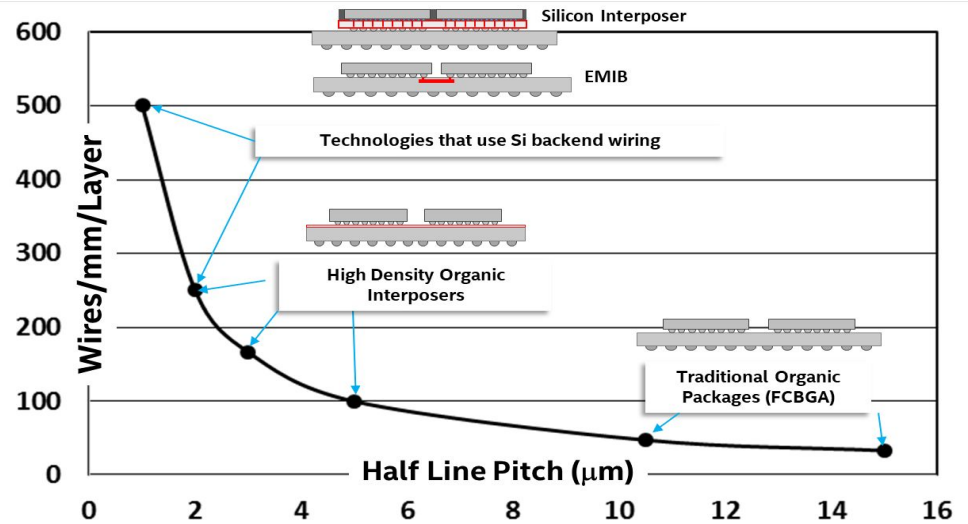
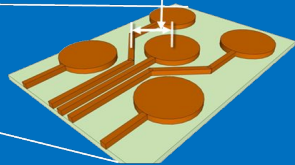
- Wiring Density increases Require Wire (aka IO) Width, Space & Pad reduction (Zero Pad Ideal)
- Bump Density Increases Require Bump Pitch Shrinks



Planar Interconnects : MCP Landscape

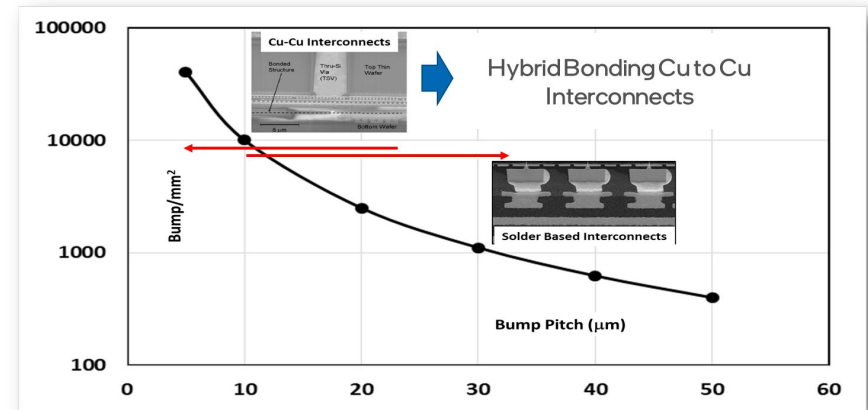
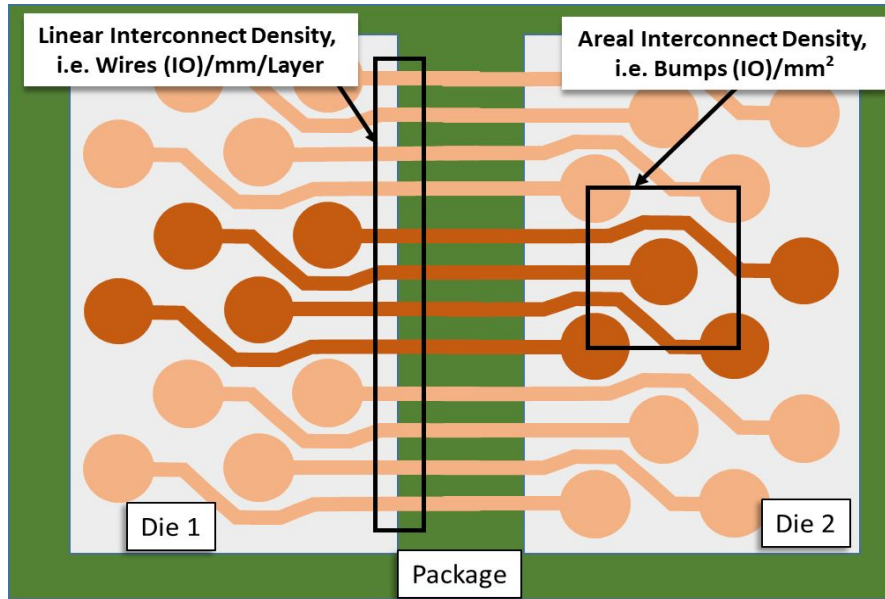


Half-Line Pitch
($\frac{1}{2}$ Line + $\frac{1}{2}$ Pad + Space)



Focus - increased
interconnect density +
Improved power efficiency
for increased BW

Vertical Interconnects : MCP Landscape

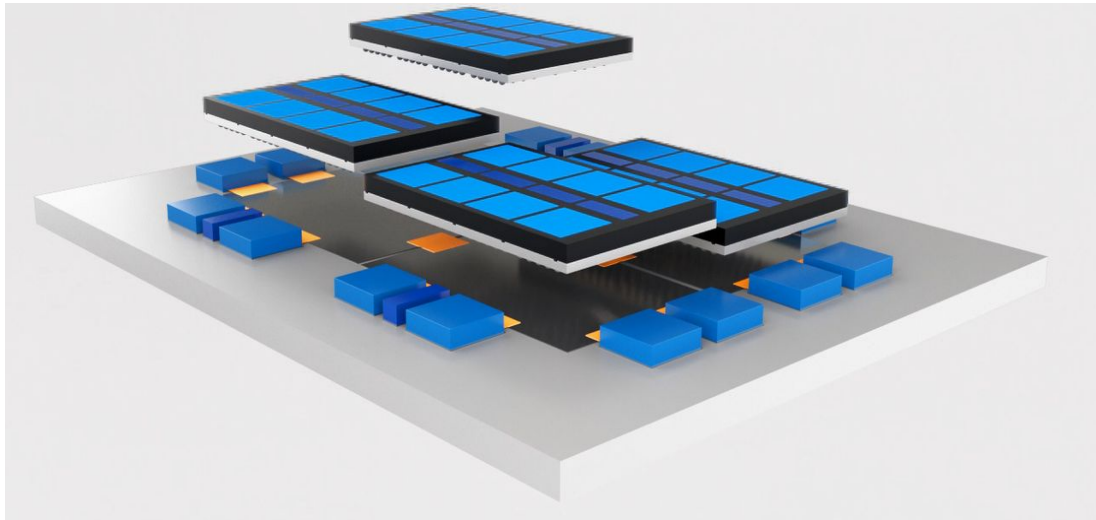
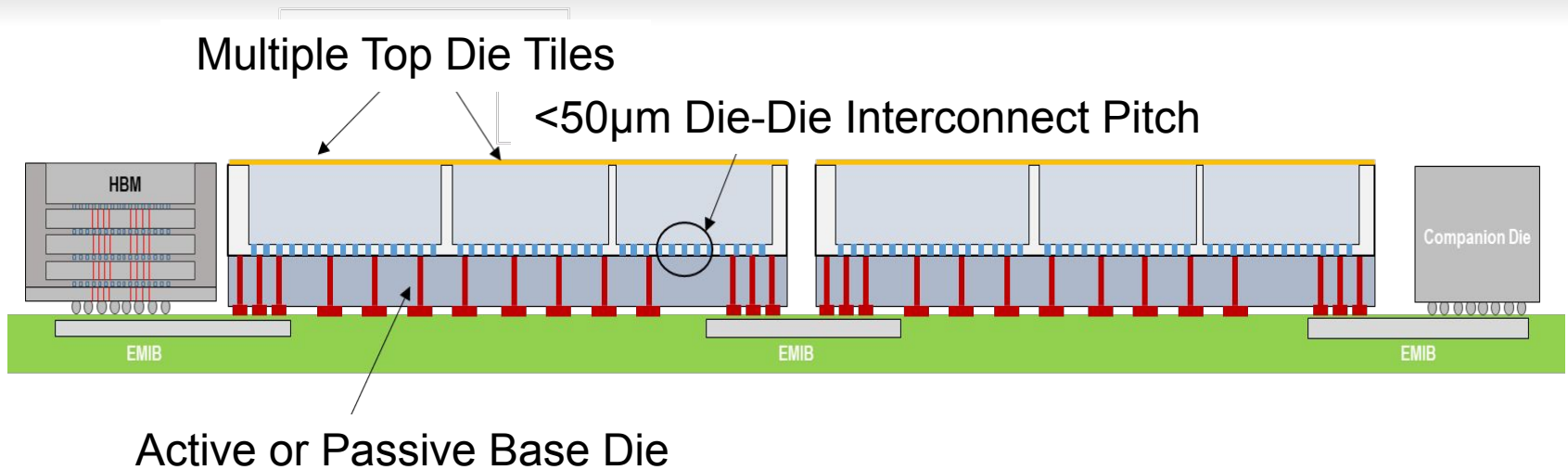


Three-Dimensional Wafer Stacking Via Cu-Cu Bonding Integrated With 65-nm Strained-Si/Low-*k* CMOS Technology

P. R. Morrow, C.-M. Park, S. Ramanathan, M. J. Koblinsky, and M. Harnes

Transition from solder based interconnects to Cu-Cu interconnects needed with shrinking bump pitch

Blending 2D and 3D



Architecture for >> reticle sized die + High-Density Bridge links increased Partitioning Opportunities in X, Y and Z

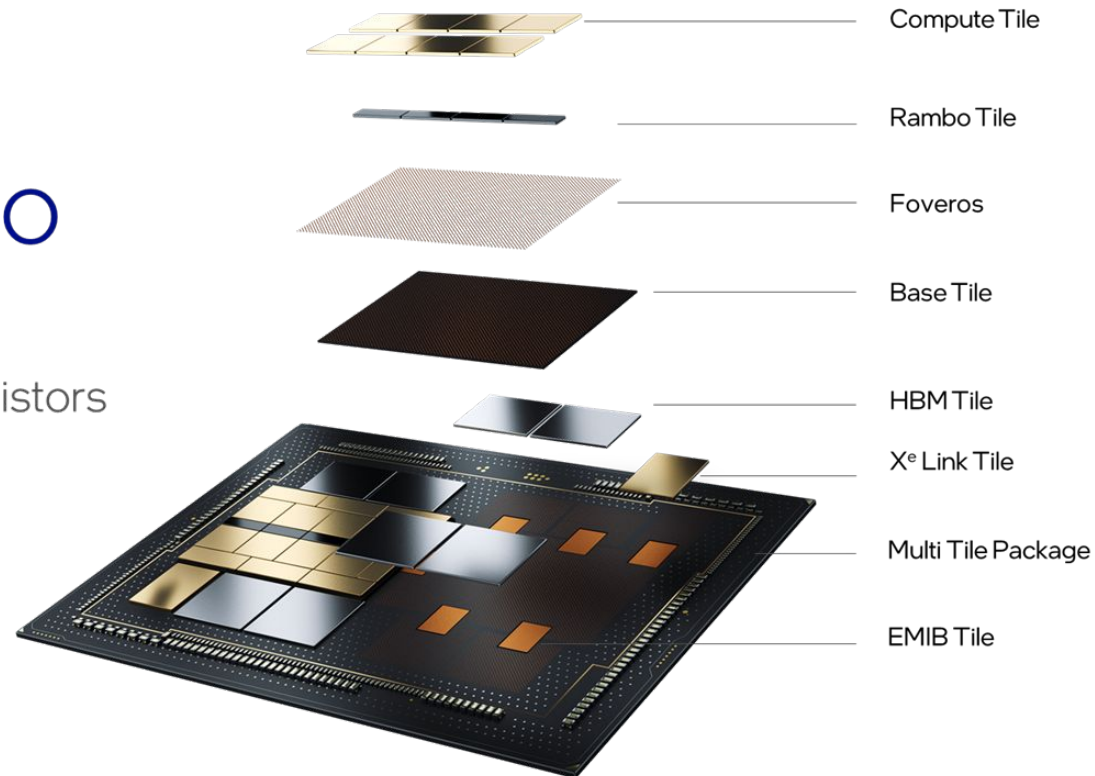
Blending Planar and 3D MCPs (EMIB + Foveros)

Ponte Vecchio soc

>100 Billion Transistors

47 Active Tiles

5 Process Nodes



Summary



- Interconnect scaling can enable complex MCPs

Disclaimer



Intel is a key contributor in the development and delivery of this course at ASU. As such, many of the charts used in our presentations are provided by Intel and are approved for use in training and educational purposes only.

The electronic industry is extremely fast-paced. We will endeavor to call out any outdated information that may be present in the presentations or texts. Regardless, the key points/learning are still valid.

